CLAIMS

1. A method of transferring digital signal packets out of a packetized memory device on a data bus, each digital signal packet including at least one packet word including a plurality of digital signals that are applied to respective latches in the packetized memory device, the method comprising:

placing the packetized memory device in a synchronization mode of operation;

generating a data clock signal responsive to a read clock signal and applying the data clock signal on a corresponding line of the data bus;

generating a plurality of internal clock signals read clock signal, each internal clock signal having a phase shift relative to the data clock signal;

storing for each digital signal a phase command in a corresponding storage circuit associated with the digital signal, the phase command having a value corresponding to one of the internal clock signals;

placing each digital signal on a corresponding data bus line responsive to the internal clock signal corresponding to the phase command stored in the associated storage circuit;

receiving a phase adjustment command corresponding to a particular digital signal that is being synchronized, the phase adjustment command containing adjustment information for the phase command associated with the digital signal;

adjusting the value of the phase command stored in the storage circuit associated with the digital signal being synchronized responsive to the phase adjustment command until the value of the phase command defines a timing offset between the digital signal and the data clock that allows and external device to successfully capture the digital signal responsive to the data clock signal; and

repeating the operations of placing each digital signal on a corresponding bus line to adjusting the value of the phase command signal for each digital signal in the packet word.

2. The method of claim 1 wherein the values of the phase commands for all the digital signals are adjusted in parallel.

3. The method of claim 1 wherein adjusting the value of the phase command stored in the storage circuit comprises reading an initial value of the phase command from the storage circuit, incrementing or decrementing the values of the initial phase command response to the phase or adjustment command, to generate a new phase command, and storing the new phase command in the storage circuit.

4. The method of claim 1 wherein each storage circuit comprises a register.

5. The method of claim 1 wherein placing the packetized memory device in the synchronization mode comprises capturing a FLAG signal and generating a calibration signal when the FLAG signal has a predetermined binary value for two consecutive captures.

6. The method of claim 1 wherein adjusting the value of the phase command stored in the storage circuit associated with the digital signal being synchronized comprises:

repetitively placing digital signals having expected values onto the corresponding data bus line;

evaluating the digital signal captured responsive to the data clock signal to determine if captured digital signal has the expected value;

identifying each phase command that caused the associated digital signal having the expected value to be captured;

selecting a phase command for each digital signal from one of the phases that caused the associated digital signal having the expected value to be captured; and

storing the selected phase command in the corresponding register.

7. The method of claim 6 wherein the operations of evaluating the captured digital signal to determine if the stored digital signal has the expected value through storing the selected phase command in the corresponding register are performed sequentially

on each of the digital signals to sequentially select a phase command associated with each digital signal.

8. The method of claim 6 wherein evaluating the captured digital signal to determine if the digital signal has the expected value comprises:

capturing the digital signal responsive to the data clock signal;

generating expected values for the digital signal responsive to the digital the values of the captured digital signal;

capturing the digital signal responsive to the data clock signal; and

determining that the digital signal was successfully captured when the values of the captured digital signal corresponds to the generated expected values for the digital signal.

9. A method of adaptively adjusting respective timing offsets of a plurality of digital signals relative to a clock signal being output along with the digital signals to enable a circuit receiving the digital signals successfully to each of the digital signals responsive to the clock signal, the method comprising:

storing in a respective storage circuit associated with each digital signal a corresponding phase command, the phase command defining a particular timing offset between the corresponding digital signal and the clock signal;

outputting the clock signal;

outputting each digital signal having the timing offset defined by the corresponding phase command;

capturing the digital signals responsive to the clock signal;

evaluating the captured digital signals to determine if each digital signal was successfully captured;

generating a phase adjustment command to adjust the value of each phase command;

repeating the operations of outputting the clock signal through generating a phase adjustment command for a plurality of phase adjustment commands for each digital signal;

selecting for each digital signal a phase command that causes the digital signal to be successfully captured; and

storing in the storage circuit associated with each digital signal the corresponding selected phase command.

10. The method of claim 9 wherein the operations of outputting a clock signal through generating a phase adjustment command are performed in parallel on all the digital signals.

11. The method of claim 9 wherein generating a phase adjustment command to adjust the value of each phase command comprises reading an initial value of the phase command from the storage circuit, incrementing or decrementing the values of the initial phase command response to the phase adjustment command, to generate a new phase command, and storing the new phase command in the storage circuit.

12. The method of claim 9 wherein each storage circuit comprises a register.

13. The method of claim 9 wherein the clock signal corresponds to a data clock signal output from a packetized memory device and each digital signal corresponds to a data signal applied on a data bus of the packetized memory device.

14. The method of claim 12 wherein outputting each digital signal having the timing offset defined by the corresponding phase command comprises outputting a repeating 15 bit pseudo-random bit sequence of "111101011001000" for each digital signal , with the timing offset of this sequence being defined by the phase command.

15. The method of claim 12 wherein capturing the digital signals responsive to the clock signal comprises capturing the digital signals responsive to the rising and falling edges of the clock signal.

16. A read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command and each register being associated with at least one of the latch circuits;

a clock generation circuit coupled to latch circuits and the phase command registers, the clock generation circuit generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock signal having a respective phase shift relative to the read clock signal, and the clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a control circuit coupled to the clock generation circuit and the phase command registers, the control circuit operable in response to a synchronization command to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the external data clock signal and the synchronization digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command register that allow the

synchronization digital signals to be successfully captured responsive to the external data clock signal.

17. The read synchronization circuit of claim 16 wherein the control circuit comprises:

a read data pattern generator that generates the synchronization digital signals, each signal being a repeating pseudo-random bit sequence;

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a phase adjustment command word responsive to adjustment signals included in the latched command-address signals, the phase adjustment command word including information identifying a particular digital signal; and

an up/down phase counter-controller coupled to the command decoder and sequencer to receive the phase adjustment command word, and coupled to the phase command registers, the counter-controller adjusting the value of the phase command stored in the register associated with the identified digital signal responsive to the phase adjustment command word.

18. The read synchronization circuit of claim 17 wherein the counter-controller adjusts the value of the phase command stored in each register by first reading a present value of the stored phase command, incrementing or decrementing the present value of the phase command responsive to the phase adjustment command to develop a new phase command word, and thereafter storing the new phase command in the register.

19. The read synchronization circuit of claim 16 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

20. The read synchronization circuit of claim 19 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

21. The read synchronization circuit of claim 16 wherein each latch circuit comprises a data latch and a buffer.

22. A memory device, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals , the read data path circuit comprising a read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock

signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command responsive to a control signal and each register being associated with at least one of the latch circuits;

a clock generation circuit coupled to latch circuits and the phase command registers, the clock generation circuit generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock signal having a respective phase shift relative to the read clock signal, and the clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a synchronization control circuit coupled to the clock generation circuit and the phase command registers, the control circuit operable in response to the initialization signals to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the external data clock signal and the synchronization digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command register that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal.

23. The memory device of claim 22 wherein the control circuit comprises:

a read data pattern generator that generates the synchronization digital signals, each bit having a repeating 15 bit pseudo-random bit sequence for the synchronization signals;

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a phase adjustment command word responsive to adjustment signals included in the latched command-address signals, the phase adjustment command word including information identifying a particular digital signal; and

an up/down phase counter-controller coupled to the command decoder and sequencer to receive the phase adjustment command word, and coupled to the phase command registers, the counter-controller adjusting the value of the phase command stored in the register associated with the identified digital signal responsive to the phase adjustment command word.

24. The memory device of claim 23 wherein the counter-controller adjusts the value of the phase command stored in each register by first reading a present value of the stored phase command, incrementing or decrementing the present value of the phase command responsive to the phase adjustment command to develop a new phase command word, and thereafter storing the new phase command in the register.

25. The memory device of claim 22 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and

having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

26. The memory device of claim 25 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

27. The memory device of claim 22 wherein each latch circuit comprises a data latch and a buffer.

28. The memory device of claim 22 wherein the memory device comprises a packetized dynamic random access memory device.

29. The memory device of claim 28 wherein the packetized dynamic random access memory device comprises an SLDRAM.

30. A memory system, comprising:

a memory device, comprising,

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals , the read data path circuit comprising a read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command responsive to a control signal and each register being associated with at least one of the latch circuits;

a clock generation circuit coupled to latch circuits and the phase command registers, the clock generation circuit generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock signal having a respective phase shift relative to the read clock signal, and the clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a synchronization control circuit coupled to the clock generation circuit and the phase command registers, the control circuit operable in response to the internal control signals to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the external data clock signal and the synchronization digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command

register that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal; and

a memory controller coupled to the memory device.

31. The memory system of claim 30 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

32. The memory system of claim 31 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

33. The memory system of claim 30 wherein each latch circuit comprises a data latch and a buffer.

34. The memory system of claim 30 wherein the memory device comprises a packetized dynamic random access memory device.

35. The memory system of claim 34 wherein the packetized dynamic random access memory device comprises an SLDRAM.

36. The memory system of claim 30 wherein the memory device comprises a double-data rate memory device and the external data clock signal comprises a data strobe signal DQS.

37. An integrated circuit adapted to receive a plurality of input signals and generate a plurality of output signals on respective, externally accessible terminals, comprising:

a circuit adapted to receive a plurality of input signals applied to respective other of the terminals and to generate a plurality of output signals on respective other of the terminals;

a read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command responsive to a control signal and each register being associated with at least one of the latch circuits;

a clock generation circuit coupled to latch circuits and the phase command registers, the clock generation circuit generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock signal having a respective phase shift relative to the read clock signal, and the clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a control circuit coupled to the clock generation circuit and the phase command registers, the control circuit operable in response to a synchronization command to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the external data clock signal and the synchronization

digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command register that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal.

38. The integrated circuit of claim 37 wherein the control circuit comprises:

a read data pattern generator that generates the synchronization digital signals, each bit having a repeating 15 bit pseudo-random bit sequence for the synchronization digital signals;

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a phase adjustment command word responsive to adjustment signals included in the latched command-address signals, the phase adjustment command word including information identifying a particular digital signal; and

an up/down phase counter-controller coupled to the command decoder and sequencer to receive the phase adjustment command word, and coupled to the phase command registers, the counter-controller adjusting the value of the phase command stored in the register associated with the identified digital signal responsive to the phase adjustment command word.

39. The integrated circuit of claim 38 wherein the counter-controller adjusts the value of the phase command stored in each register by first reading a present value of the stored phase command, incrementing or decrementing the present value of the phase command responsive to the phase adjustment command to develop a new phase command word, and thereafter storing the new phase command in the register.

40. The integrated circuit of claim 37 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

41. The integrated circuit of claim 40 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

42. The integrated circuit of claim 37 wherein each latch circuit comprises a data latch and a buffer.

43. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor, comprising,

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command responsive to a control signal and each register being associated with at least one of the latch circuits;

a clock generation circuit coupled to latch circuits and the phase command registers, the clock generation circuit generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock signal having a respective phase shift relative to the read clock signal, and the clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a synchronization control circuit coupled to the clock generation circuit and the phase command registers, the control circuit operable in response to the internal control signals to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the external data clock signal and the synchronization digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command register that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal.

44. The computer system of claim 43 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

45. The computer system of claim 44 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

46. The computer system of claim 43 wherein each latch circuit comprises a data latch and a buffer.

47. The computer system of claim 43 wherein the memory device comprises a packetized dynamic random access memory device.

48. The computer system of claim 47 wherein the packetized dynamic random access memory device comprises an SLDRAM.

49. The computer system of claim 43 wherein the memory device comprises a double-data rate memory device and the external data clock signal comprises a data strobe signal DQS.

50. A read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command and each register being associated with one of the latch circuits;

a programmable delay clock generator that develops N internal clock signals responsive to the read clock signal;

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to an associated phase command register to receive the stored phase command, and N inputs coupled to the generator to receive the N internal clocks signals, respectively, the multiplexer applying a selected internal clock signal on the output to clock the corresponding latch circuit in response to the phase command;

a read data pattern generator coupled to the inputs of the latch circuits, the generator applying a synchronization signal to each input; and

an up/down phase counter-controller coupled to the read data pattern generator and the phase command registers, the counter-controller operable to adjust the values of the phase commands stored in the registers in response to received phase adjustment command

words to thereby adjust the respective timing offsets between the external data clock signal and the synchronization signal being output by the latch circuits, and the counter-controller storing final phase commands in each phase command register that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal.

51. The read synchronization circuit of claim 50 wherein the counter-controller adjusts the value of the phase command stored in each register by first reading a present value of the stored phase command, incrementing or decrementing the present value of the phase command responsive to the phase adjustment command to develop a new phase command word, and thereafter storing the new phase command in the register.

52. The read synchronization circuit of claim 50 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

53. The read synchronization circuit of claim 50 wherein each latch circuit comprises a data latch and a buffer.

54. A read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and an external data clock signal to enable an external device to latch the digital signals responsive to the external data clock signal, the read synchronization circuit comprising:

a plurality of data storage means for storing respective signals and providing the stored signals on respective signal terminals, each data storage means storing the signal applied on an input and providing the stored signal on the corresponding signal terminal responsive to a clock signal;

a plurality of phase storage means for storing respective phase commands, each phase storage means being associated with one of the data storage means;

a clock generation means coupled to the data storage means and the phase storage means for generating a plurality of internal clock signals and the external data clock signal responsive to a read clock signal, each internal clock signal and the external clock

signal having a respective phase shift relative to the read clock signal, and the clock generation means including selection means for selecting one of the internal clock signals for each data storage means in response to the associated phase command and applying the selected internal clock signal as the clock signal to the data storage means to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a control means coupled to the clock generation means and the phase storage means for receiving a synchronization command and, in response to the synchronization command, applying a respective synchronization digital signals to each storage means and adjusting the respective timing offsets between the external data clock signal and each of the synchronization digital signals being provided on the signal terminals by each storage means by adjusting the respective values of the phase commands stored in the phase storage means, and storing final phase commands in each phase storage means that allow the synchronization digital signals to be successfully captured responsive to the external data clock signal.

55. The read synchronization circuit of claim 54 wherein the control means comprises:

a data pattern generation means for generating the synchronization digital signals, each signal being a repeating pseudo-random bit sequence;

a command buffering and address capturing means for latching command-address signals applied on a command address bus;

a command decoding and sequencing means coupled to the command buffering and address capturing means for generating a plurality of control signals responsive to the latched command-address signals, and generating a phase adjustment command word responsive to adjustment signals included in the latched command-address signals, the phase adjustment command word including information identifying a particular digital signal; and

a phase counter-controller means coupled to the command decoding and sequencing means to receive the phase adjustment command word and coupled to the phase storage means, the counter-controller means adjusting the value of the phase command stored

in the phase storage means associated with the identified digital signal responsive to the phase adjustment command word.

56. The read synchronization circuit of claim 55 wherein the counter-controller means adjusts the value of the phase command stored in each phase storage means by first reading a present value of the stored phase command, incrementing or decrementing the present value of the phase command responsive to the phase adjustment command to develop a new phase command word, and thereafter storing the new phase command in the phase storage means.

57. The read synchronization circuit of claim 54 wherein the clock generation means comprises:

a programmable delay clock generation means for generating N internal clock signals responsive to the read clock signal; and

a plurality of multiplexing means, each multiplexing means having an output coupled to a corresponding data storage means to apply the clock signal to the storage means and including a plurality of selection inputs coupled to the associated phase storage means to receive the stored phase command, and having N inputs coupled the programmable delay clock generation means to receive the N internal clock signals, each multiplexing means applying a selected one of the N internal clock signals to the clock terminal of the corresponding data storage means responsive to the phase command.

58. The read synchronization circuit of claim 57 wherein the programmable delay clock generation means comprises a delay-locked loop means.

59. The read synchronization circuit of claim 54 wherein each data storage means comprises a latching means for storing data and a buffer means coupled to the latching means for providing the stored data on the corresponding signal terminal.

60. A memory system, comprising:

a system clock generator that develops a system read data clock signal;

a memory device coupled to the clock generator to receive the system read data clock signal, comprising,

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a read synchronization circuit that adaptively adjusts respective timing offsets of a plurality of digital signals applied on respective signal terminals and the system read data clock signal to enable an external device to latch the digital signals responsive to the system read data clock signal, the read synchronization circuit comprising:

a plurality of latch circuits, each latch circuit including an input, an output coupled to a respective signal terminal, and a clock terminal, and each latch circuit storing a signal applied on the input and providing the stored signal on the signal terminal responsive to a clock signal applied on the clock terminal;

a plurality of phase command registers, each phase command register storing a phase command responsive to a control signal and each register being associated with at least one of the latch circuits;

an internal clock generation circuit coupled to latch circuits and the phase command registers, the internal clock generation circuit generating a plurality of internal clock signals responsive to the system read data clock signal, each internal clock signal and the system read data clock signal having a respective phase shift relative to the system read data clock signal, and the internal clock generation circuit selecting one of the internal clock signals for each latch circuit in response to the associated phase command and applying the selected internal clock signal to the clock terminal of the latch circuit to place digital signals on the corresponding signal terminal with a timing offset determined by the phase shift of the selected internal clock signal; and

a synchronization control circuit coupled to the internal clock generation circuit and the phase command registers, the control circuit operable in response to the internal control signals to apply synchronization digital signals on the inputs of the latch circuits and to adjust the respective timing offsets between the system read data clock signal and the synchronization digital signals output by each latch circuit by adjusting the respective values of the phase commands, and storing final phase commands in each phase command register that allow the synchronization digital signals to be successfully captured responsive to the system read data clock signal; and

a memory controller coupled to the memory device and coupled to the system read clock generator to receive the system read data clock signal.

61. The memory system of claim 60 wherein the clock generation circuit comprises:

a programmable delay clock generator that generates N internal clock signals responsive to the read clock signal; and

a plurality of multiplexers, each multiplexer having an output coupled to a respective clock terminal of a corresponding latch circuit, a plurality of selection inputs coupled to the associated phase command register to receive the stored phase command, and

having N inputs coupled the programmable delay clock generator to receive the N internal clock signals, each multiplexer applying a selected one of the N internal clock signals to the clock terminal of the corresponding latch responsive to the phase command.

62. The memory system of claim 61 wherein the programmable delay clock generator comprises a delay-locked loop circuit.

63. The memory system of claim 60 wherein each latch circuit comprises a data latch and a buffer.

64. The memory system of claim 60 wherein the memory device comprises a packetized dynamic random access memory device.

65. The memory system of claim 64 wherein the packetized dynamic random access memory device comprises an SLDRAM.

66. The memory system of claim 60 wherein the memory device comprises a double-data rate memory device and the external data clock signal comprises a data strobe signal DQS.